**Problem based on Instruction Format**

An instruction format defines the different component of an instruction. The main components of an instruction are opcode (which instruction to be executed) and operands (data on which instruction to be executed). Here are the different terms related to instruction format:

* **Instruction set size –** It tells the total number of instructions defined in the processor.
* **Opcode size –** It is the number of bits occupied by the opcode which is calculated by taking log of instruction set size.
* **Operand size –** It is the number of bits occupied by the operand.
* **Instruction size –** It is calculated as sum of bits occupied by opcode and operands.

**Que-1.** Consider a processor with 64 registers and an instruction set of size twelve. Each instruction has five distinct fields, namely, opcode, two source register identifiers, one destination register identifier, and a twelve-bit immediate value. Each instruction must be stored in memory in a byte-aligned fashion. If a program has 100 instructions, the amount of memory (in bytes) consumed by the program text is \_\_\_\_\_\_\_\_\_\_\_\_.   
(A) 100   
(B) 200   
(C) 400   
(D) 500

**Que-2.** A processor has 40 distinct instructions and 24 general purpose registers. A 32-bit instruction word has an opcode, two registers operands and an immediate operand. The number of bits available for the immediate operand field is\_\_\_\_\_\_\_.

**Que-3.** A machine has a 32-bit architecture, with 1-word long instructions. It has 64 registers, each of which is 32 bits long. It needs to support 45 instructions, which have an immediate operand in addition to two register operands. Assuming that the immediate operand is an unsigned integer, the maximum value of the immediate operand is \_\_\_\_\_\_\_\_\_\_\_.

**Que-4.** A processor has 16 integer registers (R0, R1, …, R15) and 64 floating point registers (F0, F1, … , F63). It uses a 2-byte instruction format. There are four categories of instructions: Type-1, Type-2, Type-3, and Type 4. Type-1 category consists of four instructions, each with 3 integer register operands (3Rs). Type-2 category consists of eight instructions, each with 2 floating point register operands (2Fs). Type-3 category consists of fourteen instructions, each with one integer register operand and one floating point register operand (1R+1F). Type-4 category consists of N instructions, each with a floating point register operand (1F).

The maximum value of N is \_\_\_\_\_\_\_\_

Que-5 Top of Form

Bottom of Form

Top of Form

Que-5 In a 10-bit computer instruction format, the size of address field is 33-bits. The computer uses expanding OP code technique and has 44 two-address instructions and 16 one-address instructions. The number of zero address instructions it can support is

1. 256
2. 356
3. 640
4. 756

Que-6 Match list I with List II and select the correct answer using the codes given below the lists.

Table

Description automatically generated

Que-7 A stack organized computer has which of the following instructions?

1. zero-address
2. one-address
3. two-address
4. three-address

Que-8 For computer based on three-address instruction formats, each address feild can be used to specify which of the following:  
(S1) A memory operand  
(S2) A processor register  
(S3) An implied accumulator register

1. Either S1 or S2
2. Either S2 or S3
3. Only S2 and S3
4. All of S1, S2 and S3

Que-9. The instruction ADD 3030 is of

* 1. 3-address instruction format
  2. 2-address instruction format
  3. 1-address instruction format
  4. 0-address instruction form

Q10. For a 0-address instruction format, what would be the top element of the stack following sequences of instructions?

PUSH 20;

PUSH 5;

PUSH 5;

ADD;

SUB;

PUSH 20;

MUL.

1. 100
2. 200
3. 10
4. 5

Solution-1: It can be approached as:   
The instruction consists of opcode and operands.

Given the instruction set of size 12, 4 bits are required for opcode (2^4 = 16).   
As there are total 64 registers, 6 bits are required for identifying a register.   
As the instruction contains 3 registers (2 source + 1 designation), 3 \* 6 = 18 bit are required for register identifiers.   
12 bits are required for immediate value as given.   
Total bits for an instruction = 4 + 18 + 12 = 34 bits   
The instructions are required to be stored in a byte-aligned fashion. The nearest byte boundary after 34 bits is at 40 bits (5 bytes).  
Hence, for 100 instructions, the memory required is 5 \* 100 = 500 bytes, and the correct option is (D).